WHAT IS CLAIMED IS:

1. A path transistor circuit comprising:

a plurality of path transistors connected in parallel and each one having input terminals, same input signal is being inputted into said input terminals of said path transistors, and continuities of the plurality of said path transistors is being controlled by a plurality of control signals having an exclusive relationship therebetween; and

a plurality of buffers which drive drive segments including at least said path transistors and wirings, the drive segments being a plurality of divided ranges each having an equal potential.

2. The path transistor circuit according to claim 1, wherein each of said buffer has a driving force capable of driving a necessary, sufficient load capacity with a reference to the worst value of the load capacity of said drive segments.

3. The path transistor circuit according to claim 1, wherein said buffers are provided corresponding to a part of said drive segments.

4. The path transistor circuit according to claim 1, wherein said path transistor circuit being used as a bit shift circuit applying the select logic of the path transistors and operating output bits relative to input bits.

5. A path transistor circuit design method comprising:

a first step of designing a plurality of path transistors connected in parallel and having input terminals, respectively, into which input terminals a same input signal is inputted, continuities of the plurality of path transistors controlled by a plurality of control signals having an exclusive relationship therebetween; and

a second step of designing a plurality of buffers respectively driving drive segments including at least the plurality of path transistors and wirings, the drive segments being a plurality of divided ranges each having an equal potential.

6. A logic circuit optimization device for optimizing design of a logic circuit consisting of a plurality of path transistors connected in parallel and having input terminals, respectively, into which input terminals a same input signal is inputted, said logic circuit optimization device comprising:

a logic specification indication unit which indicates

logic specifications so that a plurality of control signals controlling continuities of the plurality of path transistors, respectively, have an exclusive relationship therebetween;

a cell library unit which registers a plurality of cell data used to design said logic circuit; and

an optimization unit which conducts a logic composition based on the logic specifications and the cell data, and for optimizing buffering in said logic circuit.

7. The logic circuit optimization device according to claim 6 further comprising a grouping unit which groups said path transistors into a plurality of groups based on the exclusive relationship,

wherein said optimization unit conducts logic composition based on said grouped drive segments, the logic specifications and the cell data, and optimizes buffering in said logic circuit.

8. The logic circuit optimization device according to claim 7 wherein said optimization unit optimizes buffering with respect to a part of said drive segments.

9. The logic circuit optimization device according to claim 6, wherein said logic circuit is a bit shift circuit applying the select logic of the path transistors and operating output bits relative to input bits.

10. The logic circuit optimization device according to claim 6, wherein a plurality of the logic circuits are provided to constitute a macro circuit.

11. The logic circuit optimization device according to claim 6, wherein a first cell data applying the maximum value of the load capacity of said logic circuit and a second cell data applying the minimum value of the load capacity are registered, as cell data for analyzing the electric characteristics of the logic circuit, in said cell library unit.

12. The logic circuit optimization device according to claim 11, wherein the first and second cell data are created according to the actual operation of said logic circuit.

13. A logic circuit optimization method for optimizing design of a logic circuit consisting of a plurality of path transistors connected in parallel and having input terminals, respectively, into which input terminals a same input signal

is inputted, the method characterized by comprising:

a logic specification indication step of indicating logic specifications so that a plurality of control signals respectively controlling continuities of the plurality of path transistors have an exclusive relationship therebetween;

a registration step of registering a plurality of cell data used to design said logic circuit in a cell library; and

an optimization step of conducting logic composition based on the logic specifications and the cell data and optimizing buffering in said logic circuit.

14. A computer-readable recording medium recording a logic circuit optimization program applied to a logic circuit optimization device for optimizing design of a logic circuit consisting of a plurality of path transistors connected in parallel and having input terminals, respectively, into which input terminals a same input signal is inputted, the computer-readable recording medium characterized by recording the logic circuit optimization program to allow a computer to execute:

a logic specification indication step of indicating logic specifications so that a plurality of control signals respectively controlling continuities of the plurality of

path transistors have an exclusive relationship therebetween;

a registration step of registering a plurality of cell data used to design said logic circuit in a cell library; and

an optimization step of conducting logic composition based on the logic specifications and the cell data and optimizing buffering in said logic circuit.